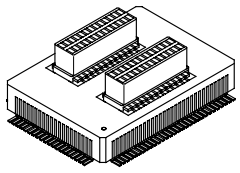
SONY

CXP921000A

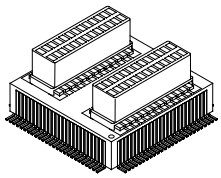
CMOS 16-bit Single Chip Microcomputer

Piggy/ evaluation type

100 pin PQFP (Ceramic)



(QFP supported)



(LQFP supported)

Description

The CXP921000A is a CMOS 16-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP921064A.

Features

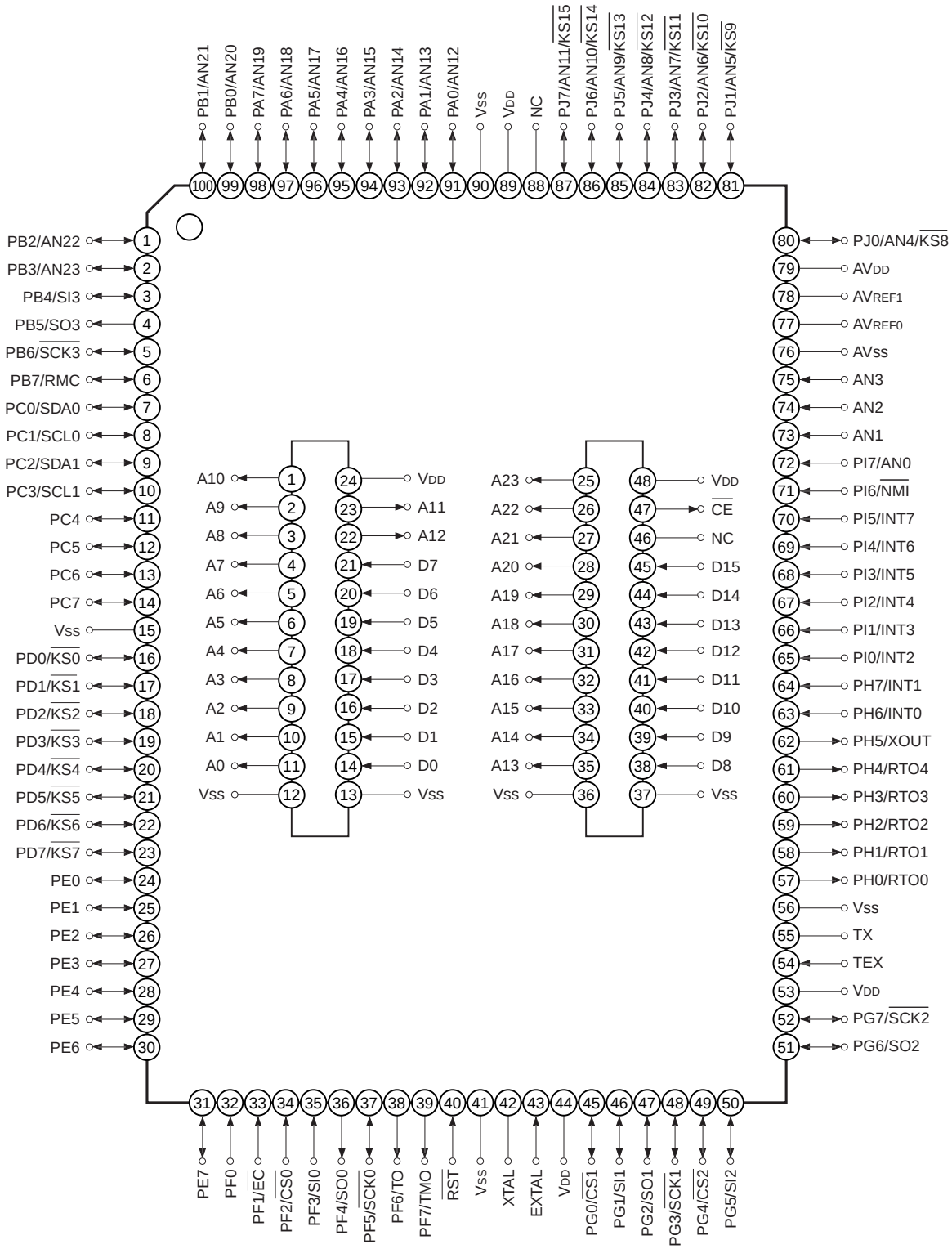
- An efficient instruction set as a controller
  - Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - Highly quadratic instruction system, general-purpose register of eight 16-bit × 16-bank configuration
- Minimum instruction cycle time 100ns at 20MHz operation (2.7 to 3.3V)
  61µs at 32kHz operation (2.2 to 3.3V)
- Incorporated EPROM CXP27V1000K
- Incorporated RAM capacity 10K bytes
- Peripheral functions
  - — A/D converter 8-bit 12 analog input, 2 channels successive approximation system, automatic scanning function, (Conversion time: 3.4µs at 20MHz)
  - — Serial interface 128 -byte buffer RAM, 3 channels
    8-stage FIFO, 1 channel (supports special mode master/slave)
  - — I^2C bus interface 64-byte buffer RAM , 2 channels
    (supports master/slave and automatic transfer mode)
  - — Timers 8-bit timer/counter, 2 channels (with timing output)
    16-bit timer, 3 channels
  - — Real-time pulse generator 5-bit output, 1 channel (2-stage FIFO)
  - — Clock prescaler
  - — Remote control receive circuit 8-bit pulse measurement counter, 8-stage FIFO
- Interruption 30 factors, 30 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin Ceramic PQFP
- Mask ROM CXP921064A
- FLASH EEPROM incorporated type CXP921F064A

Structure

Silicon gate CMOS IC

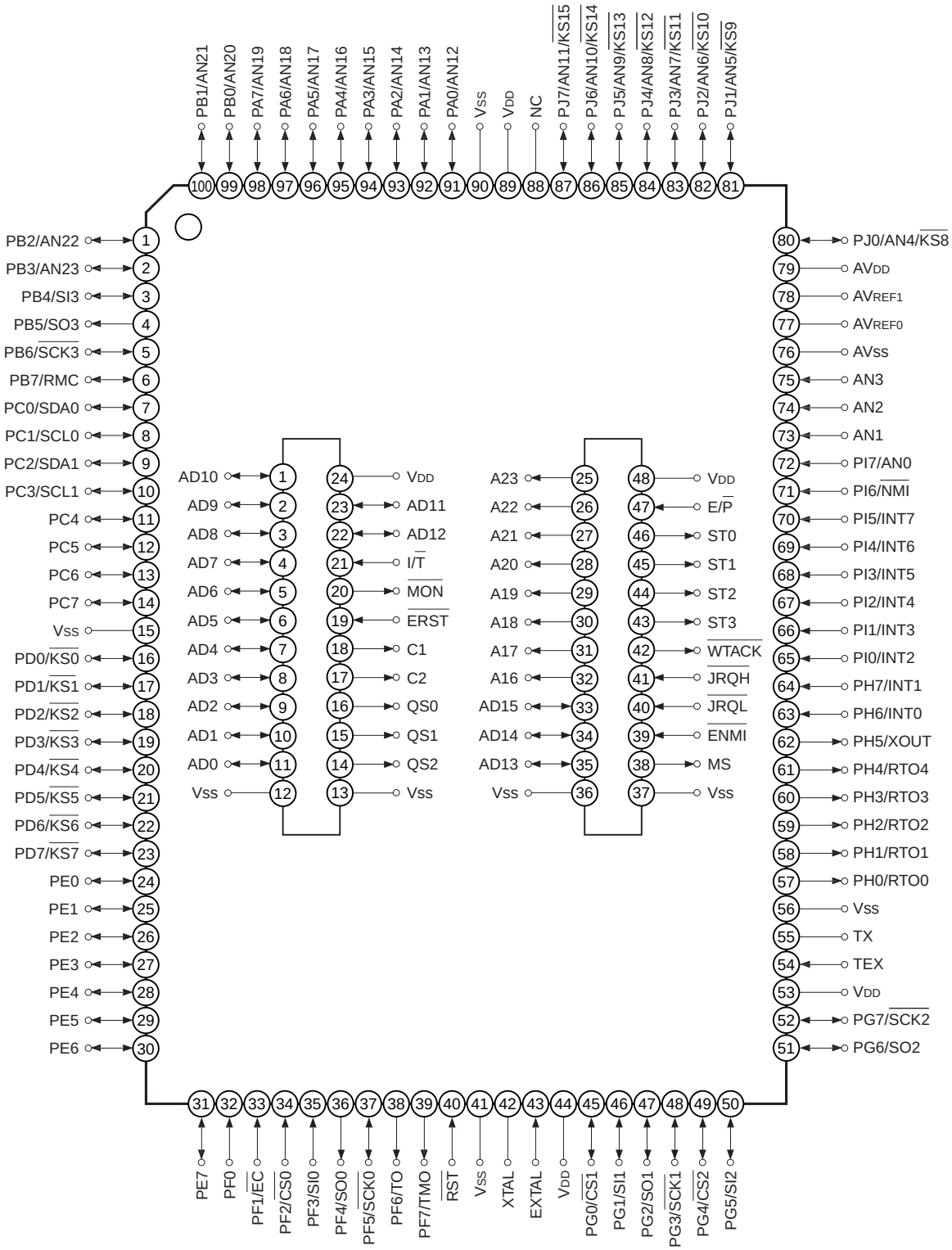
E99X11-PS

Pin Assignment in Piggyback Mode (Top View) 100-pin QFP package



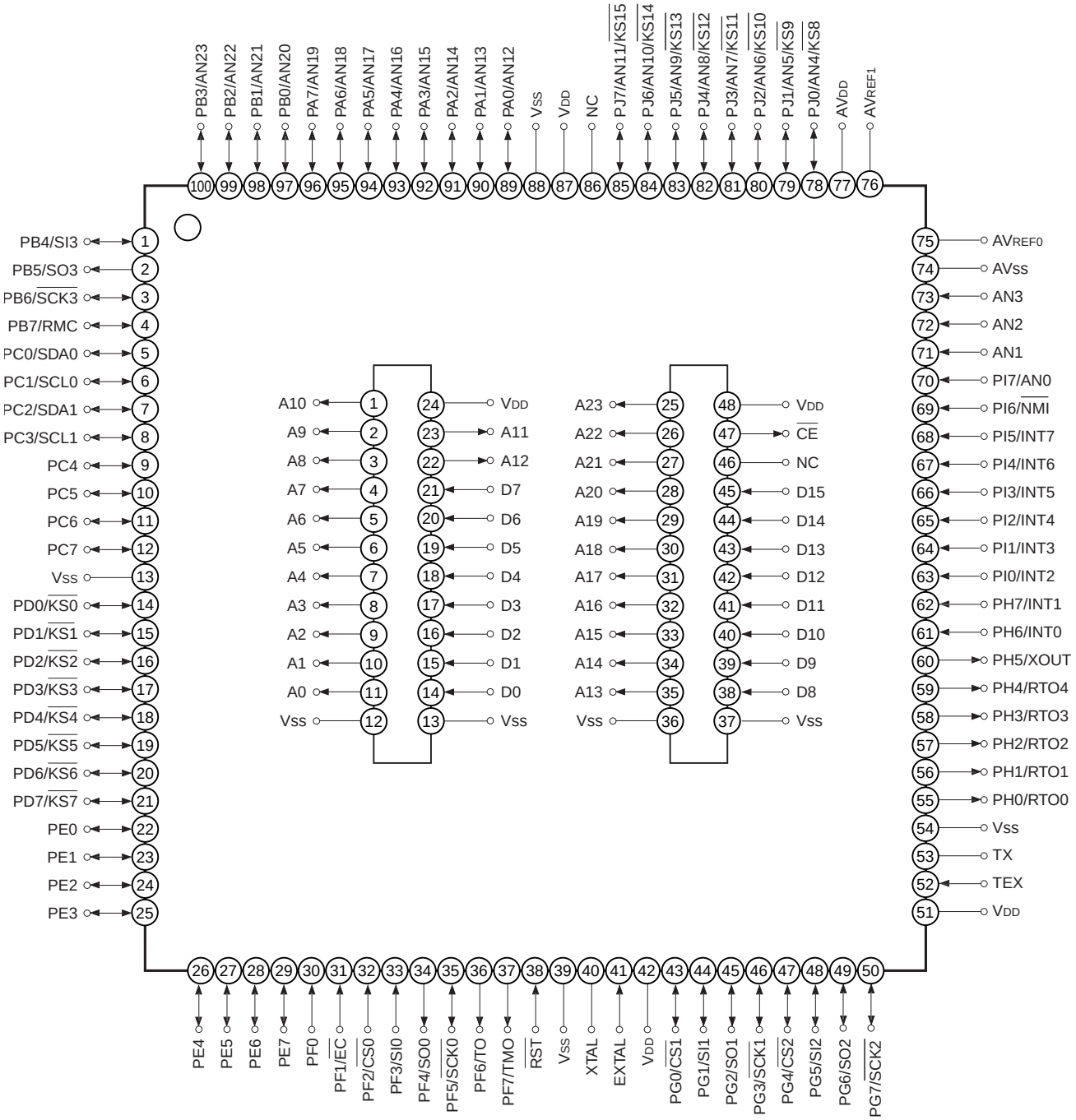
Note) 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss (Pins 15, 41, 56 and 90) must be connected to GND.
3. VDD (Pins 44, 53 and 89) must be connected to VDD.
4. A20 to A23 are always high level output.

Pin Assignment in Evaluator Mode (Top View) 100-pin QFP package



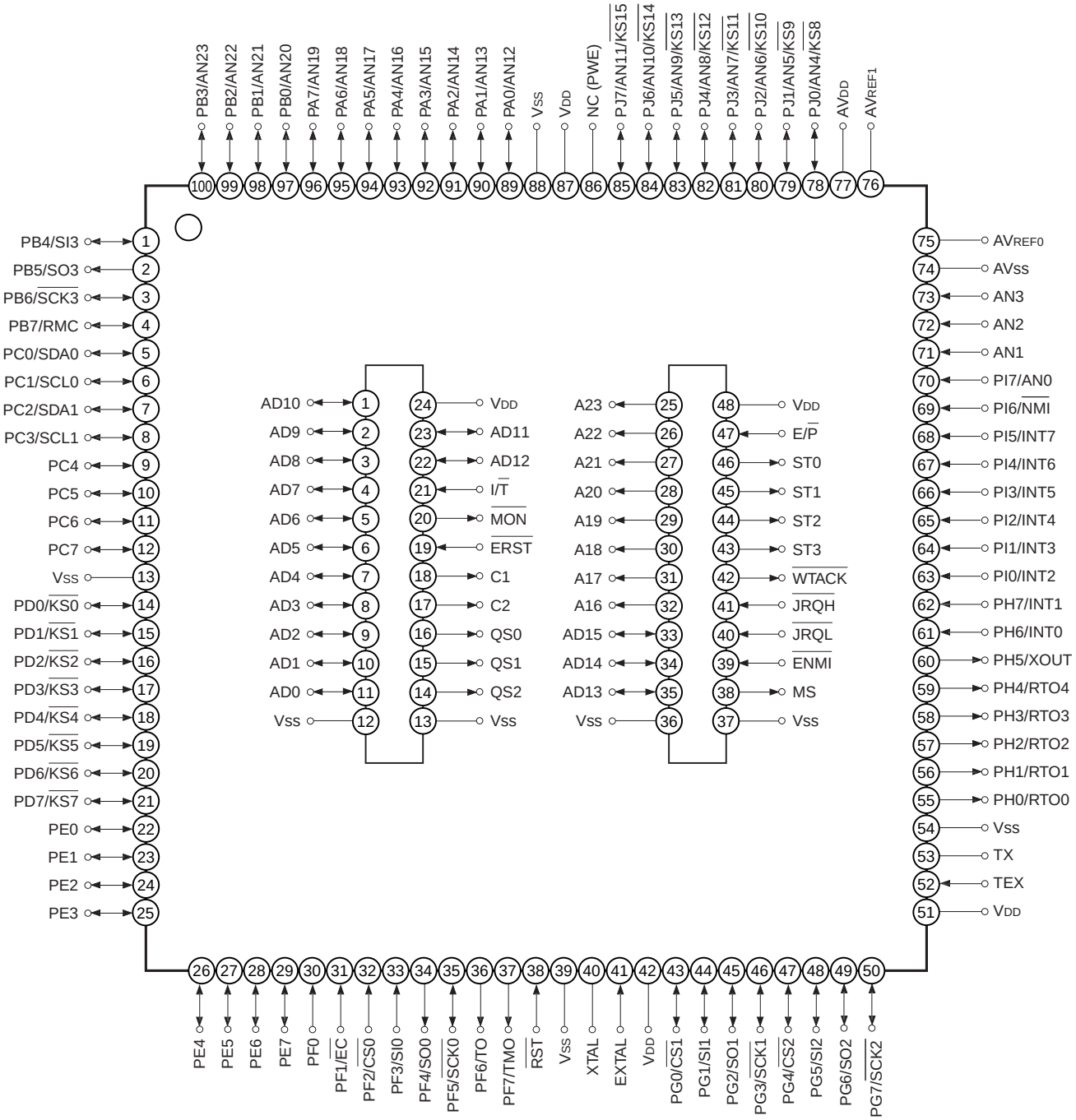
Note) 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss (Pins 15, 41, 56 and 90) must be connected to GND.
3. V_{DD} (Pins 44, 53 and 89) must be connected to V_{DD}.

Pin Assignment in Piggyback Mode (Top View) 100-pin LQFP package



Note) 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss (Pins 13, 39, 54 and 88) must be connected to GND.
3. VDD (Pins 42, 51 and 87) must be connected to VDD.
4. A20 to A23 are always high level output.

Pin Assignment in Evaluator Mode (Top View) 100-pin LQFP package

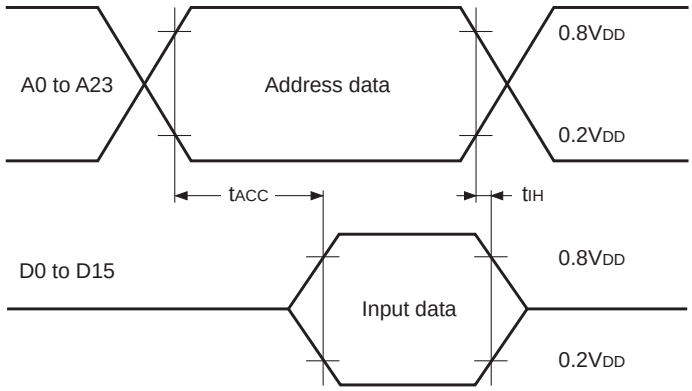


Note) 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss (Pins 13, 39, 54 and 88) must be connected to GND.
3. VDD (Pins 42, 51 and 87) must be connected to VDD.

EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V)

Item	Symbol	Pins	Min.	Max.	Unit
Address → data Input delay time	t_{ACC}	A0 to A23 D0 to D15		50	ns
Address → data hold time	t_{IH}	A0 to A23 D0 to D15	0		ns



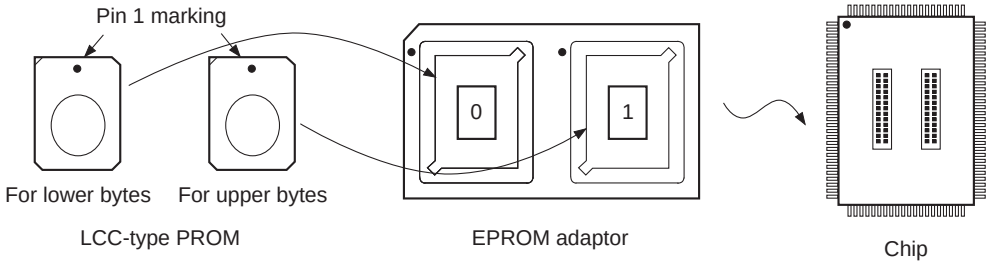
Product List

Optional item	Products		
	Mask ROM	Piggy/evaluation chip	
	CXP921064A	CXP921000A-U01Q	CXP921000A-U01R
Package	100-pin plastic QFP/LQFP 104-pin plastic LFLGA	100-pin ceramic PQFP (QFP supported)	100-pin ceramic PQFP (LQFPsupported)
ROM capacity	256K bytes	EPROM 256K bytes	
Reset pin pull-up resistor	Existent/Non-existent	Existent	

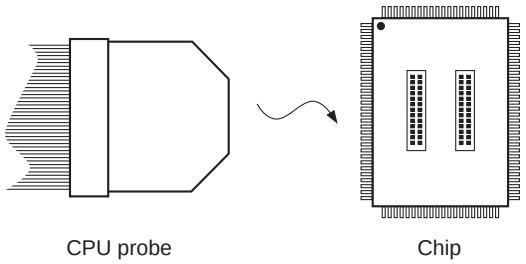
Switching of Piggyback Mode and Evaluator Mode

Piggyback mode can be used by setting two LCC-type EPROM (for upper bytes, for lower byte) and connecting to the connector of top of the chip.
Evaluator mode can be used by connecting in-circuit emulator CPU probe to the connector of top of the chip.

Piggyback mode



Evaluator mode

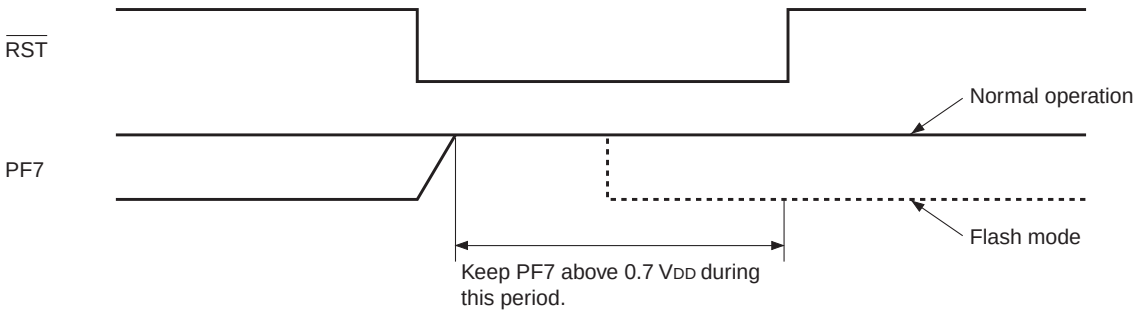


Notes on PF7 Usage

FLASH EEPROM incorporated PF7 is also used as flash mode setting function. Note the followings:

1. "H" is output to PF7 during a reset. That is driven at comparatively high impedance (approximately 150kΩ), and take care that V_{OH} should not fall under $0.7V_{DD}$ by the partial pressure with external circuit load impedance.

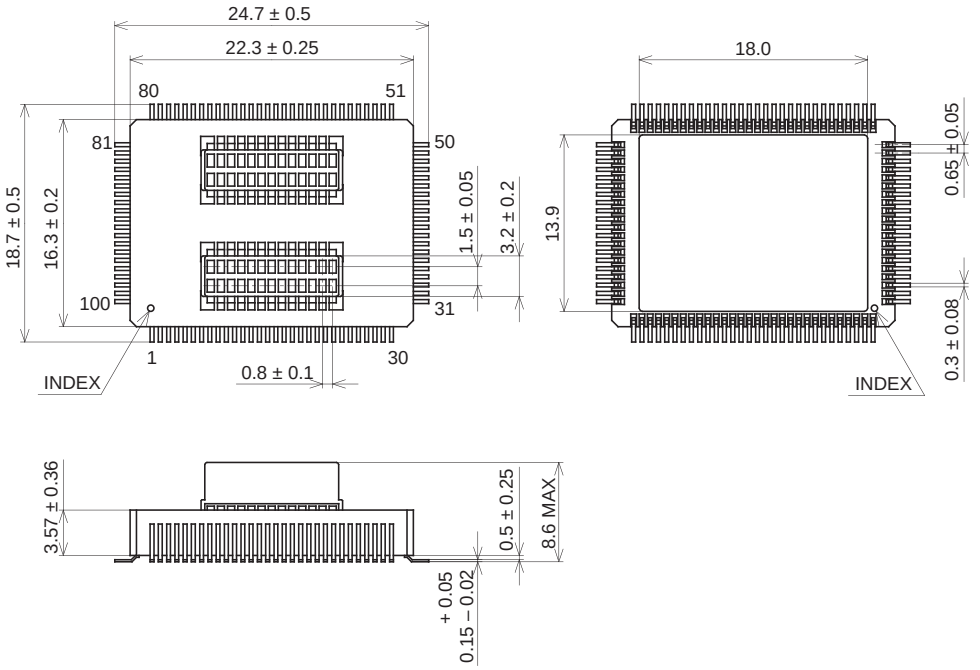
2. When using software reset functions, PF7 may not rise enough during a reset. Switching PF7 to "H" output prior to software reset execution or connecting pull-up resistor is recommended.



Mask ROM and piggy/evaluation chip do not have flash mode setting function. Considering that EEPROM incorporated type is used, above countermeasure should be performed.

Package Outline Unit: mm

100PIN PQFP(CERAMIC)

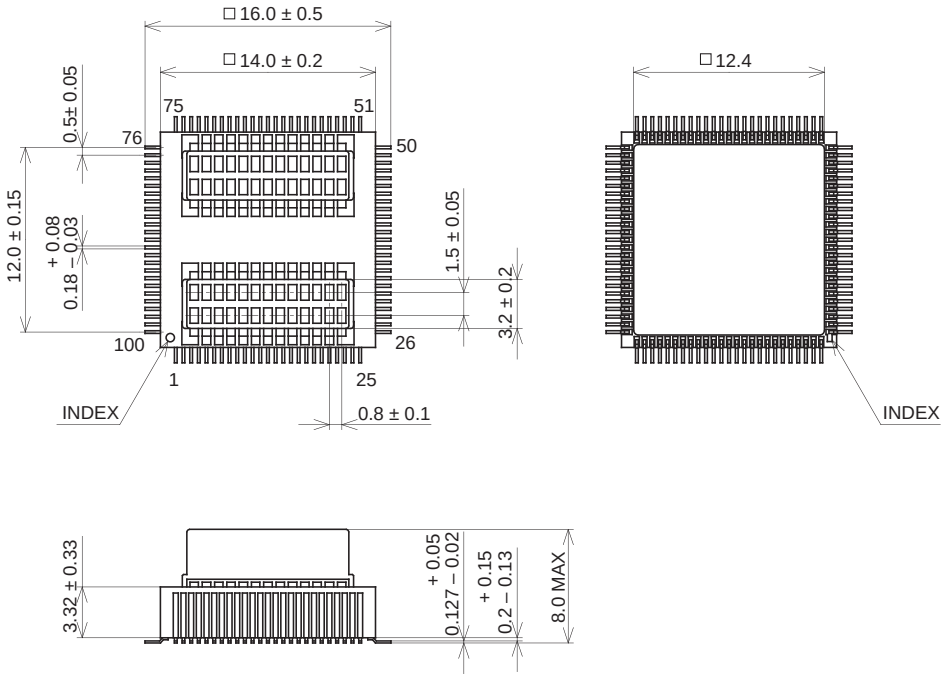


SONY CODE	PQFP-100C-L04
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	4.9g

100PIN PQFP(CERAMIC)



SONY CODE	PQFP-100C-L03
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.7g